

Floure 1

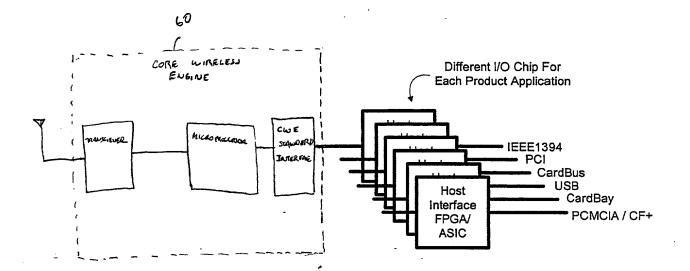


FIGURE 2

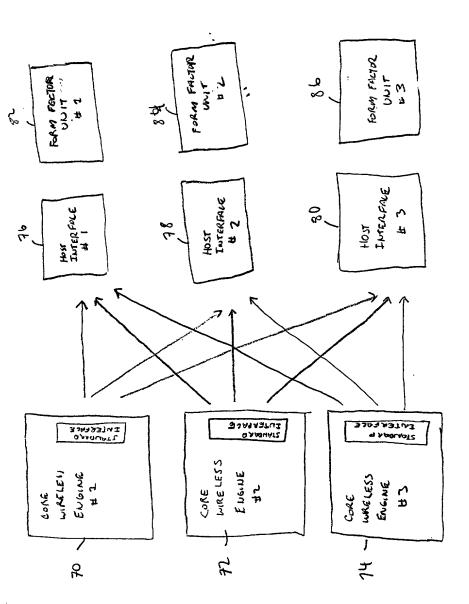


FIGURE 3

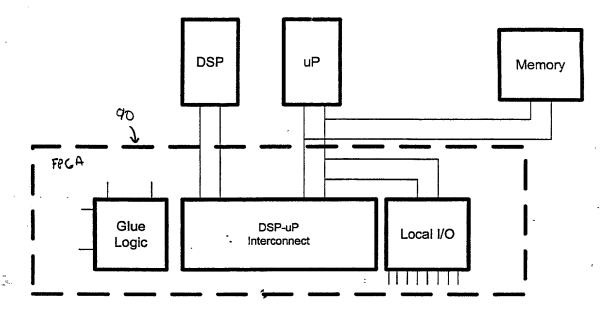


FIGURE 4A

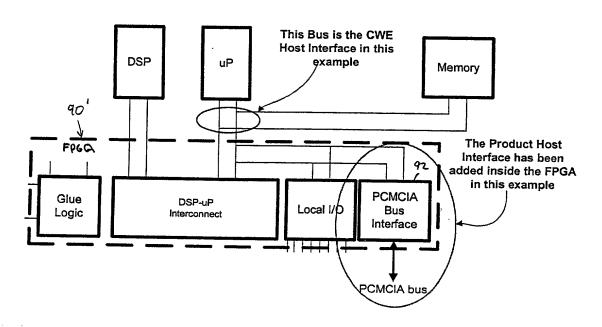
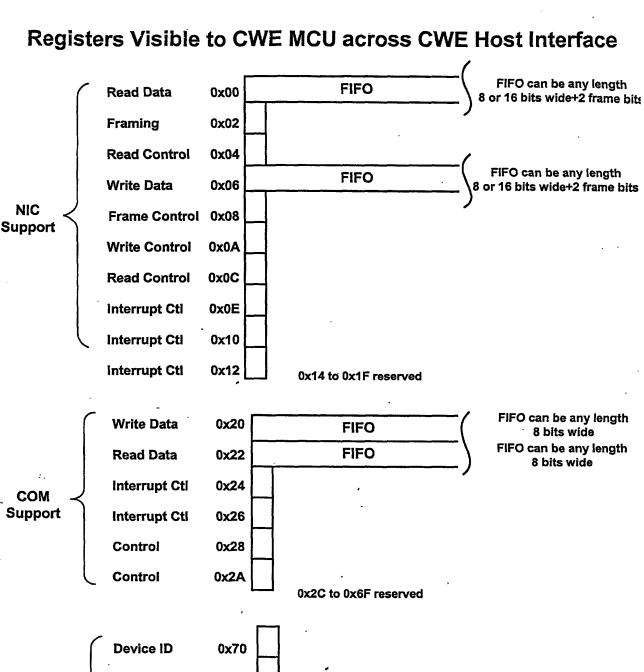
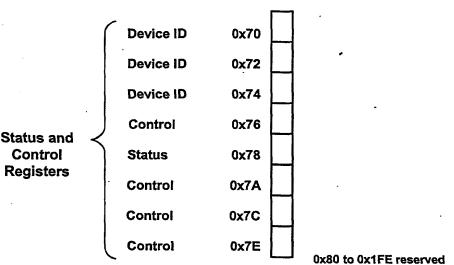


FIGURE 4B





We do the man has

F160RE 5

CWE Host Interface A0 Α1 A2 Address А3 A4 Α5 A6 D0 Host D1 D2 **CWE** D3 I/O FPGA/ Data D4 **ASIC** D5 D6 D7

Read Strobe

CS Chip Select Strobe

IRQ Interrupt Request

WR Write Strobe

FIGURE 6

RD

RESET

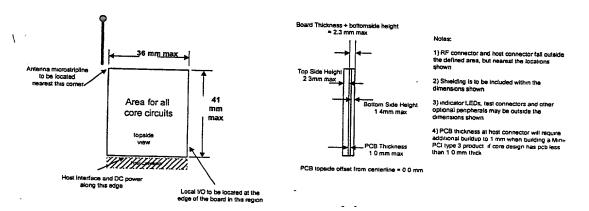


FIGURE 7

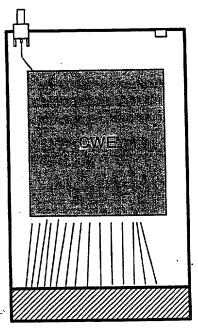


FIGURE 8A

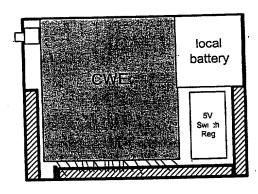
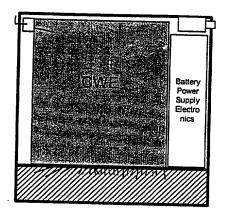


FIGURE 8C



FIGURE 8E



FIBURE 8B

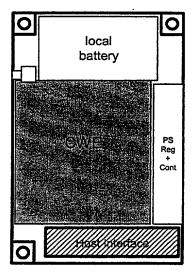


FIGURE 80

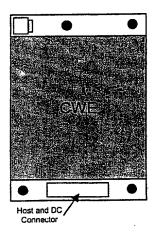


FIGURE 8 F